53. A description language model of an integrated circuit design generated using the method comprising:

obtaining user input information;

identifying at least one library file;

generating a script using said said library file and user input information; and

running said script to create said description language model of said integrated circuit design.

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54. An integrated circuit, comprising:

a processor core; and

a memory operatively coupled to said microprocessor;

wherein said integrated circuit is designed using the method comprising:

selecting the cache size;

determining the memory interface configuration;

selecting at least one customized instruction;

identifying at least one library;

generating a script based at least on said cache size, memory interface configuration, at least one customized instruction, and said library; and

running said script to create a customized hardware description language model of the design.

55. A system for generating integrated circuit designs, comprising:

a processor;

a storage device in data communication with said processor, said storage device being capable of storing and retrieving a computer program; and

a computer program stored within said storage device and adapted to run on said processor, said computer program comprising;

a user-configurable macro-instruction having at least a first user-selectable element, said first-selectable element being selected from the group consisting of;

(i) a plurality of custom instructions;

(ii) a plurality of cache configurations;

(iii) a plurality of memory interface configurations; and

(iv) a plurality of system architecture configurations;

a first algorithm capable of generating a script based on selections made by a user from said at least first user selectable element; and

a second algorithm capable of running said script to generate a description language model of an integrated circuit design.

56. A data storage device, comprising:

storage media capable of storing a plurality of data files; and

a computer program stored on said data storage media, said computer program comprising:

a user-configurable macro-instruction having at least one user-selectable element, said user-selectable element being selected from the group consisting of;

(i) a plurality of instructions;

(ii) a plurality of cache configurations;

(iii) a plurality of memory interface configurations; and

(iv) a plurality of system architecture configurations;

a first algorithm capable of generating a script based on selections made by said user from said user-configurable macro-instruction; and

a second algorithm capable of running said script to generate a description language model of an integrated circuit design.

57. A method of generating the design of an integrated circuit using a hardware description language, comprising the acts of:

selecting a process technology;

editing first data specific to the design, said act of editing comprising selecting at least one user-configurable parameter selected from the group consisting of;

(i) processor instructions;

(ii) cache configuration;

(iii) memory interface configuration; and

(iv) system architecture configuration;

identifying at least one library;

generating a script using said first data and said library; and

running said script to create a customized hardware description language model of the design.

58. A sub-micron feature integrated circuit, comprising:

a microprocessor core having a program bus and data bus;

at least one cache memory; and

a random access memory (RAM) operatively coupled to said microprocessor;

wherein said integrated circuit is created using the following steps performed interactively during the design process:

selecting the size of said cache;

defining the configuration of the interface with said RAM;

selecting at least one customized instruction performed by said microprocessor core;

identifying at least one library;

generating a script based at least on said size of said cache, said RAM interface configuration, said at least one customized instruction, and said at least one library; and

running said script to create a customized hardware description language model of the design;

wherein said microprocessor core, said program and data busses, said RAM, and said cache are all physically located on the same die.

59. An integrated circuit, fabricated using the method comprising:

obtaining user input specific to a desired integrated circuit design;

identifying at least one library;

generating a script using at least said user input and said library;

running said script to create a customized description language model of said integrated circuit design;

generating a netlist which is descriptive of the circuitry of said integrated circuit;

compiling said netlist and said hardware description model to produce a compiled integrated circuit design;

compiling at least one configuration file, and

fabricating said integrated circuit using at least said configuration file.

60. A method of designing a configurable processor, the method comprising:

generating a processor specification having a user-definable portion, the user-definable portion of said specification including at least one user-defined instruction having a function associated therewith; and

based on said processor specification, generating a description of a hardware implementation of said configurable processor.

61. The method of Claim 60, wherein said act of generating a description comprises generating a description including control logic necessary for the execution of said at least one user-defined instruction.

62. The method of Claim 61, wherein said act of generating a description of a hardware implementation comprises describing at least an instruction execution pipeline having a plurality of stages, said control logic including portions associated with said stages.

63. The method of Claim 60, wherein said act of generating a description comprises generating a description having at least one element selected from the group consisting of:

(i) registers;

(ii) condition code choices; and

(iii) scratchpad RAM.

64. The method of Claim 60, wherein said act of generating a description comprises generating a description having at least one library of multimedia extensions.

65. The method of Claim 60, further comprising simulating said configurable processor using at least said description.

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66. The method of Claim 65, wherein said act of simulating comprises:

running at least one script to generate simulation data;

running at least one simulation using at least said simulation data; and

determining the adequacy of said configurable processor based at least in part on said act of running.

67. The method of Claim 60, further comprising synthesizing said configurable processor using at least said description.

68. The method of Claim 67, wherein said act of synthesizing comprises:

running at least one synthesis script to generate synthesis data;

and evaluating the adequacy of said synthesis data based at least in part on at least one design criterion.

69. The method of Claim 68, wherein said at least one design criterion comprises:

at least one specific processor performance criterion; and

at least one processor die size criterion.

70. The method of Claim 68, further comprising:

revising at least one design element when said act of evaluating indicates that said synthesis data is not adequate;

re-running said at least one synthesis script using said at least one revised design element to generate revised synthesis data;

and re-evaluating the adequacy of said revised synthesis data based at least in part on said at least one design criterion.

71. The method of Claim 70, wherein said at least one design criterion comprises at least one processor die size criterion, and said act of revising comprises revising at least one library.

72. The method of Claim 71, wherein said at least one design criterion comprises at least one processor die size criterion, and said act of revising further comprises revising at least one control file.

73. The method of Claim 70, wherein said at least one design criterion comprises processor clock speed, and said act of revising comprises revising at least one library.

74. The method of Claim 70, wherein said at least one design criterion comprises processor power consumption, and said act of revising comprises revising at least one netlist (net load).